DISCUSSION OF CLAIM AMENDMENTS

Claims 20 and 29 both earlier included the limitation that layers or memory device are included in a three dimensional memory array. Both claims have been amended to include the limitation that the three dimensional memory array comprises memory cells disposed at numerous levels above a substrate. Support for this claim amendment is found in paragraph [0034], which is amended in this paper. This amendment does not constitute new matter.

DISCUSSION OF SPECIFICATION AMENDMENTS

Paragraph [0034] of the specification was amended to include the phrase "which describes a three dimensional memory array including memory cells formed at numerous levels above a substrate" when referring to US Patent Application No. 09/560,626, which was fully incorporated by reference. In the Background of the Invention, US Patent Application No. 09/560,626 characterizes three dimensional memory arrays this way. As this amendment is merely restating material incorporated by reference, this specification amendment does not constitute new matter.

REMARKS

A. Status of the Claims

Claims 1-31 are pending in the application. Claim 4 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of US Patent No. 6,635,556 (hereinafter the '556 patent) in view of Hsu, US Patent No 6,613,626. Claims 19 and 24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of the '556 patent.

Claims 1, 3-5, 15, 25, 27-28, and 30-31 were rejected under 35 USC 102(b) as being anticipated by Su, US Patent No. 5,837,582. Claims 6, 16-18, 20-23, and 29 were rejected under 35 USC 103(a) as being unpatentable over Su in view of Hill, US Patent No. 6,384,466. Claims 2 and 26 were rejected under 35 USC 103(a) as being unpatentable over Su in view of Hsu. Claims 7-14 were allowed.

Claims 3-19 and 28 are cancelled in this response.

B. Obviousness-Type Double Patenting Claim Rejections: Claims 4, 19, and 24

Claim 4 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 of the '556 patent (the parent of the present application) in view of Hsu. Claims 19 and 24 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of the '556 patent. Claims 4 and 19 are cancelled in this response.

Claim 24 recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure vessel over a surface of a product wafer substrate material while introducing a precursor gas; and without removing

the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the first doped silicon layer, wherein the layers form a portion of a three dimensional memory array, the three dimensional memory array comprising memory cells disposed at numerous levels above a substrate; further comprising forming a second doped layer on and in contact with the undoped capping layer, wherein the first doped layer is formed with n-type or p-type dopants and the second layer is formed with n-type or p-type dopants, the type of the second layer opposite the type of the first layer. (This summary includes the limitations of claim 24, and those of claims 21 and 20, from which it depends.)

Claim 1 of the '556 patent recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure vessel over a surface of a product wafer substrate material while introducing a precursor gas, the first doped layer comprising n-type or p-type silicon; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on the first doped silicon layer, the undoped silicon capping layer having a thickness sufficient to reduce autodoping to approximately a background level; and forming a next doped silicon layer on the undoped silicon capping layer, the next doped layer comprising p-type or n-type silicon, the type opposite the type of the first doped layer.

The Examiner maintains that the scope of claim 1 of the '556 patent encompasses the scope of claim 24 of the present invention. Applicant respectfully points out, however, that claim 24 includes the limitation that the first doped layer and the undoped

capping layer form a portion of a three dimensional memory array. No such limitation appears in claim 1 of the '556 patent.

Applicant maintains, then, that the limitations of claim 24 of the present invention are not taught or suggested by claim 1 of the '556 patent and respectfully request reconsideration.

C. 35 USC 102(e) Claim Rejections: Claims 1, 3-5, 25, 27-28, and 30-31

Claims 1, 3-5, 15, 25, 27-28, and 30-31 were rejected under 35 USC 102(b) as being anticipated by Su.

Claims 3-5, 15, and 28 have been cancelled.

Claim 1 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the doped silicon layer; and removing the undoped silicon capping layer.

Applicant will show that the claim includes at least two limitations that are not taught in Su: 1) the substrate material is necessarily removed from the pressure vessel between deposition of the doped layer and the undoped capping layer of Su, and 2) the undoped capping layer of Su is not removed.

The claim calls for the undoped capping layer to be deposited on the first in situ doped layer *without removing the substrate material from the pressure vessel.*

The Examiner is correct that doped layer 11a of Su is doped in situ. After deposition of layer 11a, however, at col. 3 lines 62-66, Su describes:

> An anisotropic RIE procedure, using Cl2 as an etchant, is next employed to remove polysilicon from the top surface of insulator layer 9, creating polysilicon plug structure 11a ...

In short, to form polysilicon plug 11a, insulator layer 9 is formed, and an etch is performed to form a contact hole 10 in insulator layer 9 (col. 3, lines 44-58). In situ doped polysilicon is deposited to fill contact hole 10. This deposition step is not selective, however, so while in situ doped polysilicon fills contact hole 10, it is simultaneously deposited on the top of insulator layer 9. The overfill of polysilicon on top of insulator layer 9 is undesired in the finished device, so an RIE (reactive ion etch) step is performed to remove the polysilicon overfill, leaving only plug 11a. This RIE step is performed after deposition of the first doped polysilicon layer, and before deposition of the undoped capping layer.

In the claim, the undoped capping layer is deposited *without removing the substrate material from the pressure vessel.* The precursor gas (phosphine in this case) is turned off, and the deposition of silicon with no dopant continues.

In contrast, in Su an RIE step is performed between deposition of the doped silicon layer and deposition of the undoped capping layer. Reactive ion etching cannot be performed in a chamber used to deposit silicon. One skilled in the art would assume that after deposition of doped polysilicon layer 11a, the wafer was removed from the pressure vessel, moved to a reactive ion etcher where the REI step is performed, then returned to the pressure vessel for another, separate deposition step.

In addition, undoped capping layer 11b is not removed in Su. The Examiner says that Su et al describes "etching/removing" the undoped capping layer 11b. With respect, Applicant must protest that "etching" and "removing" are not equivalent. Layer 11b of Su is etched, but it is not removed.

It is conventional in fabrication of integrated circuits to deposit a layer covering the entire wafer, as a blanket, then to subject that deposited layer to a photolithographic step, leaving only the portions of the layer that are desired in the finished device. After deposition, undoped polysilicon layer 11b of Su is patterned and etched, leaving behind layer 11b in the finished device, as shown in Figs. 5 and 6. Applicants will respectfully maintain that if layer 11b is present in the finished device, as these figures show, it cannot be said to have been removed, as required by the claim.

Applicant has shown that claim 1 distinguishes over Su. Claim 25 similarly includes the limitation that the undoped silicon capping layer is removed, and thus also distinguishes over the teachings of Su. Applicant respectfully requests reconsideration of independent claims 1 and 25, and of dependent claims 27, and 30-31, which depend from claim 25.

D. 35 USC 103(a) Claim Rejections: Claims 6, 16-18, 20-23, and 29

Claims 6, 16-18, 20-23, and 29 were rejected under 35 USC 103(a) as being unpatentable over Su in view of Hill. Claims 6 and 16 18 have been cancelled.

Claim 20 recites a method of making a silicon-based electronic device comprising the steps of: forming a first doped silicon layer in a pressure vessel over a surface of a product wafer substrate material while introducing a precursor gas; and without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the first doped silicon layer, wherein the layers form a portion of a three dimensional memory array, the three dimensional memory array comprising memory cells disposed at numerous levels above a substrate.

Applicant explained in Section C of this response that Su does not teach that the substrate material is removed from the pressure vessel before deposition of the undoped capping layer. The Examiner relies on Su for this teaching, so Applicant has already shown that each and every limitation of the claim is not taught or suggested in the combined references.

In addition, as amended, claim 20 includes the limitation that the layers form a portion of a three dimensional memory array, the three dimensional memory array comprising memory cells *disposed at numerous levels above a substrate*. Three dimensional memory arrays are fully described in Johnson et al., US Patent No. 6,034,882; and in Knall, US Patent Application No. 09/560626, both of which are fully incorporated by reference in paragraph [0034] of the instant application. A three dimensional memory array includes memory cells formed at numerous levels above a substrate; for example, as described in both Johnson et al. and Knall, a three dimensional memory array includes stacked memory levels formed above a substrate.

To find evidence of a three dimensional memory array, the Examiner refers to the following passage in Hill:

> FIG. 1 is a cross-sectional view of an assembly 10 including a number of structures 12 defining gaps or openings 18 formed on a substrate 8 and covered with a multi-layer dielectric 2 including a first dielectric layer 14 and a second dielectric layer 16. The assembly 10 may be, for example, a portion of an integrated circuit, such as a portion of a memory array or a logic circuit, as may be used to form devices, such as memories and processors.

The memory cells of Hill are clearly shown formed *in* rather than *above* the substrate, and all formed on the same level, rather than at numerous levels. Hill does not teach a three dimensional memory array.

As amended, claim 29 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on the doped silicon layer; and consuming or removing the undoped silicon capping layer, wherein the semiconductor device is a memory device, wherein the memory device is a portion of a three dimensional memory array, the three dimensional memory array comprising memory cells disposed at numerous levels above a substrate. (This summary includes the limitations of claim 29 and of claim 25, from which it depends.)

Applicant has already shown that Su shows neither forming of the undoped silicon capping layer *without removing the substrate material from the pressure vessel* nor removal of the undoped silicon capping layer, and thus that claim 29 distinguishes over the teachings of Su relied upon for this rejection. In addition, Hill does not show a memory device that is a portion of a three dimensional memory array, the three dimensional memory array comprising memory cells disposed at numerous levels above a substrate.

Applicant has shown that all of the limitations of claim 20 and its dependent claims 21-23, and of claim 29, are neither taught nor suggested by the references. Applicant points out that, while both claim 20 and claim 29 have been amended, this amendment was for clarification, and was not necessary to distinguish over the references.

E. 35 USC 103(a) Claim Rejections: Claims 2 and 26

Claims 2 and 26 were rejected under 35 USC 103(a) as being unpatentable over Su in view of Hsu.

Claim 2 recites a method of making a semiconductor device comprising: forming a first in-situ doped silicon layer over a substrate material in a pressure vessel while introducing a precursor gas; without removing the substrate material from the pressure vessel, discontinuing introduction of the precursor gas and forming an undoped silicon capping layer on and in contact with the doped silicon layer; and removing the undoped silicon capping layer, wherein the undoped silicon capping layer is removed by CMP.

In this rejection the Examiner again relies on Su to show that the undoped capping layer is formed without removing the substrate material from the pressure vessel, and that the undoped capping layer is removed. Applicant has shown that Su does not in fact teach either limitation.

In addition, the Examiner points to Hsu for the teaching of removal of the undoped capping layer by CMP:

> One skilled in the art at the time the invention was made would have found it obvious to modify Su method by removing the undoped polysilicon layer by CMP as per Hsu because Hsu discloses that polysilicon needs to be removed by CMP ...

Applicants respectfully point out, however, that Hsu does not teach removing an undoped polysilicon capping layer from on top of a doped silicon layer, as in claim 2. Hsu only teaches removing an undoped polysilicon from on top of silicon dioxide.

In preferred embodiments of Hsu, the undoped silicon layer (46 and 47) is grown by *selective* epitaxial growth of undoped silicon. (Fig. 8, and col. 6, lines 42-43.) During epitaxial growth of silicon, a thin layer of single-crystal silicon is deposited on a single-

crystal silicon substrate; epitaxial growth occurs in such way that the crystallographic structure of the silicon substrate is reproduced in the epitaxially grown silicon layer. This selective growth causes undoped epitaxially grown silicon layers 46 and 47 to form *only* over monocrystalline silicon regions 42 and 44. In this preferred epitaxial embodiment, no unwanted undoped silicon layer forms over insulation regions 36, 38, and 40 (which are formed of silicon dioxide, a dielectric material), and thus does not need to be removed.

In the less preferred embodiment to which the Examiner refers (col. 6, lines 43-48) the layer of undoped polysilicon is non-selectively deposited instead of being selectively grown epitaxially. Because the deposition is *non-selective*, an undoped silicon forms not only in layers 46 and 47, where it is intended, but also forms on top of isolation regions 36, 38, and 40. The CMP step of line 47 removes polysilicon *only* above isolation regions 36, 38, and 40; undoped silicon layers 46 and 47 on doped silicon regions 42 and 44 remain.

An element of claim 2 missing from either Su or Hsu is removing an undoped polysilicon layer *from on top of an in situ doped first layer*. The Examine finds this teaching in Hsu, suggesting that removal of an undoped polysilicon layer from silicon dioxide in Hsu makes obvious removing the undoped polysilicon layer deposited on a first doped silicon layer in Su, which, as Applicant has noted, is not in fact removed.

The undoped polysilicon layers of Hsu and of Su are in different locations, serving different purposes. The undoped polysilicon layer of Hu is removed, while the undoped polysilicon layer of Su is not removed. If the CMP method of Hu were used on the undoped silicon capping layer 11b of Su, this entire layer would in fact be removed,

and layer 11b, which is necessary for the device of Su to function, would no longer be present, rendering the device inoperable. The references cannot be combined.

Applicant has shown that the proposed combination does teaches neither a) deposition of the undoped polysilicon layer without removing the substrate material from the pressure vessel nor b) removal of the undoped capping layer; and further that a) there is no motivation to combine the references, and that b) the references cannot be combined. Claim 26 distinguishes over the proposed combination of Su and Hsu for the same reasons.

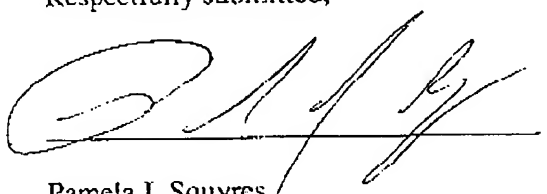
Applicant respectfully requests reconsideration of claims 2 and 26.

CONCLUSION

In light of this response, Applicants believe this application to be in condition for allowance. If there are any questions concerning this response, the Examiner is invited to contact the undersigned agent at (408) 869-2921.

Dated: December 14, 2005

Respectfully submitted,



Pamela J. Squyres
Agent for Applicants
Reg. No. 52,246

Matrix Semiconductor
3230 Scott Blvd
Santa Clara, CA 95054
Tel. 408-869-2921